

# AB-X36CXXX-X Series PECL/LVPECL HF VCXO

Rev. M

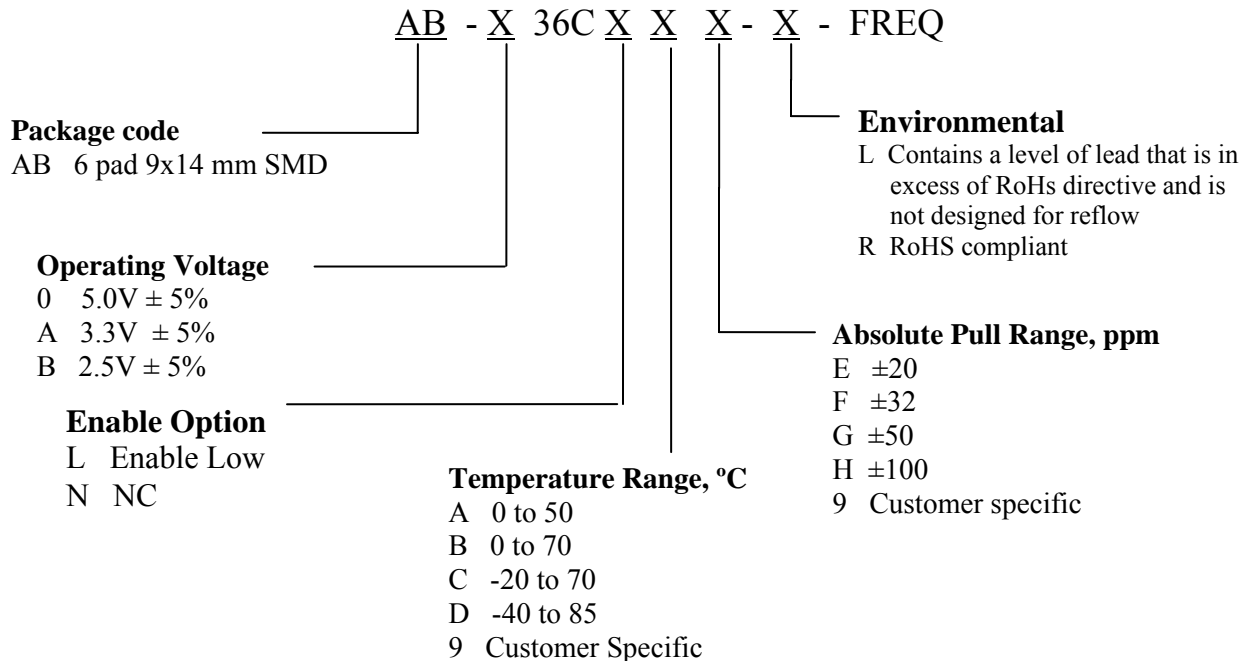
## Description

The **AB-X36CXXX Series** of voltage controlled crystal oscillators (VCXO) provides high frequency with PECL/LVPECL complementary outputs. The outputs can be disabled for test automation or combining multiple clocks. The device does not use any frequency multiplication, providing exceptionally low Phase Noise and Jitter and wide pull. It is packaged in a miniature, FR-4 based 9x14 mm SMD package

## Applications and Features

- Wide frequency range – 12.0MHz to 280.000MHz
- Fiber Channel; 10 GbE; Infiniband; Network Processors; SONET/SDH
- High Reliability – NEL HALT/HASS qualified for crystal oscillator start-up conditions
- Extremely Low Phase Noise and Jitter
- High Shock Resistance, to 1000g
- No Multiplication
- Absolute Pull Range (APR) to ±1000 ppm
- SONET ± 20 ppm overall free-run stability available
- COTS/Dual use

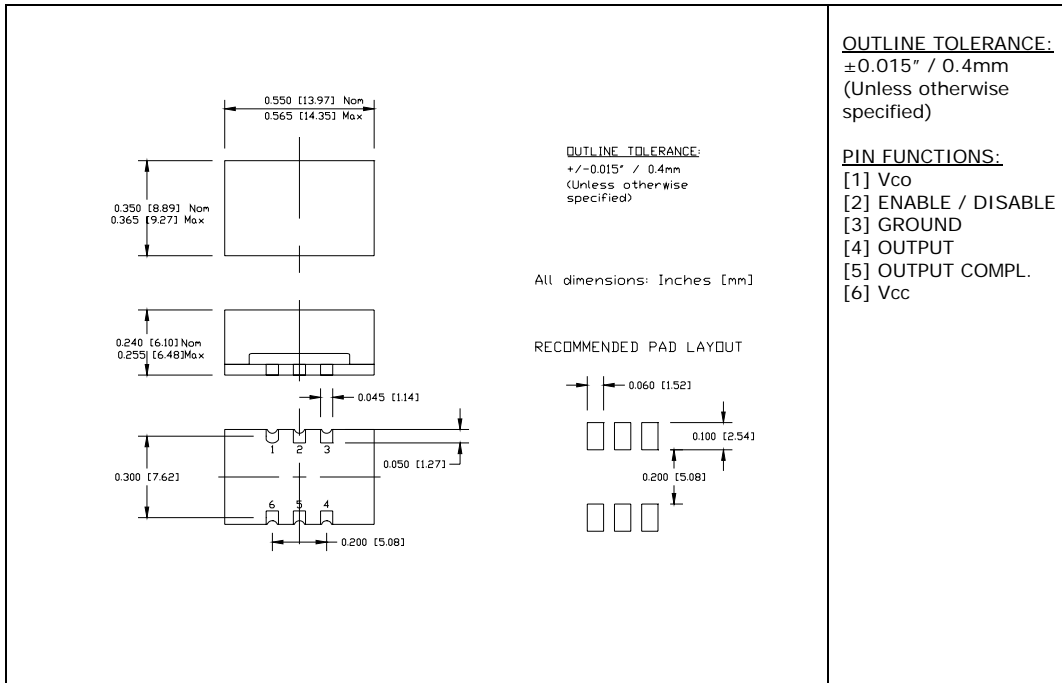
### Creating a Part Number



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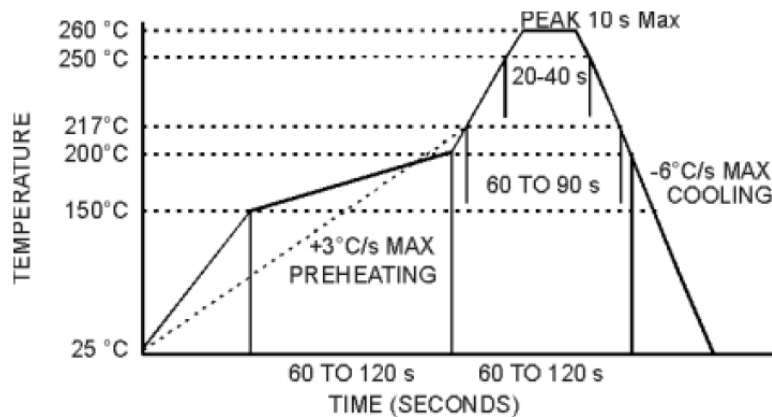
**Drawing Specification**



**Environmental and Mechanical Characteristics**

<b>Operating temp. range</b>	see part # table
<b>Mechanical Shock</b>	Per MIL-STD-202, Method 213, Cond. A
<b>Thermal Shock</b>	Per MIL-STD-883, Method 1011, Cond. A
<b>Vibration</b>	Per MIL-STD-883, Method 2007, Cond. A
<b>Hermetic Seal</b>	Leak rate less than $1 \times 10^{-8}$ atm.cc/s of helium .
<b>Soldering conditions</b>	See MAX reflow profile below; The device may be reflowed once. Reflowing upside down is not allowed. NO CLEAN assembly is recommended

**MAX Reflow Profile**



The device may be reflowed once. Reflowing upside down is not allowed. NO CLEAN assembly is recommended

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## Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Operating Temperature Range	To	-40 to +85	°C
Storage Temperature Range	Tst	-50 to +90	°C
Supply Voltage	Vcc	-0.5 to 5.5	V
Enable/Disable Voltage	Ven/dis	0 to Vcc	V

## Electrical Parameters

Parameter	Symb	Conditions, Note	MIN	TYP	MAX	Unit	
Nominal Frequency	Fo		12		280	MHz	
Supply Voltage	Vcc	Code 0 Code A Code B	4.75 3.135 2.375	5.0 3.3 2.5	5.25 3.465 2.625	V	
Supply current	Icc			60	80	mA	
Output Logic Type				LVPECL			
Load		Output to Vcc-2V, or Thevenin Equivalent		50		Ohm	
Output Levels	Voh Vol	Overall	Vcc-1.025		Vcc-1.620	V	
Duty Cycle (Symmetry)		At 50% of output voltage swing	45/55	50/50	55/45	%	
Rise/Fall Time	Tr/Tf	20 to 80, 80 to 20 %		0.5	0.7	ns	
<b>Jitter</b>	Integrated	J	Integrated from Phase Noise, 12 KHz to 20 MHz, RMS		0.1	0.2	ps
			10Hz to 80KHz,RMS			1.0	ps
			50 KHz to 80 MHz		0.3		ps
	Wavecrest characterized	J	Random period,		2.5		ps
			Accumul., pk- to-pk		17		ps
			Deterministic		0		ps
Phase Noise	£(Δf)	155.52MHz, @ 10 Hz @100 Hz @1 KHz @10KHz @100KHz @>1MHz		-75 -105 -128 -142 -147 -147	-70 -100 -125 -140 -145 -145	dBc/Hz	
Sub-harmonics			None			dBc	
Frequency Stability Usually not specified unless necessary. APR is specified to incorporate stability	ΔF/F	Overall, including temperature, aging 10 years, shock and vibration @ Vc=Vcc/2; APR 50ppm, or less	±20	±30		ppm	
Control Voltage Range	Vc		0V		Vcc	V	
Setability	Vcs	Vc to set F at Fo; T, Vcc, load – nominal as shipped	0.4 Vcc	0.5 Vcc	0.6 Vcc	V	
Absolute Pull Range	APR	Overall conditions, see part # creation	20,32, 50,100			ppm	
Input Impedance	Zin	@ Fmod < 100kHz	50			KOhm	
Modulation Bandwidth		At Vc = Vcc/2, -3dB	20			KHz	
Enable		Pin 2 = Low, 0 to Vcc-1.62V or floating	Enabled			V	
Disable		Pin 2 = High, Vcc-1.025V to Vcc	Disabled, Pin 4 = Logic "1", Pin 5 = Logic "0"			V	