

AA-A3DDXXX-X Series LVDS VCXO

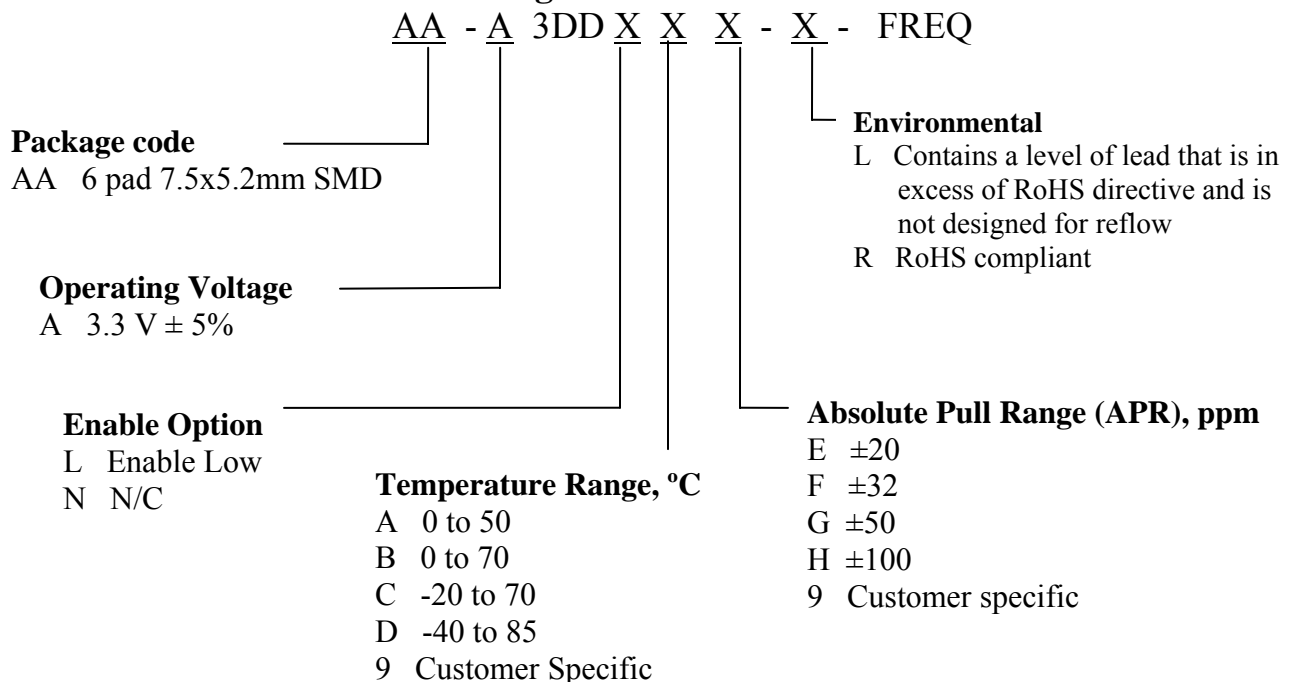
Description

The AA-A3DDXXX Series of crystal oscillators (XO) provides low phase noise LVDS complementary outputs. The outputs can be disabled for test automation or combining multiple clocks. The device packaged in a miniature, low profile, leadless FR-4 based package with gold plated pads, which enhances compatibility with PCB material.

Applications and Features

- Low Phase Noise
- Wimax, Fiber Channel; 10 GbE; Infiniband; Network Processors; SOHO Routing
- High Reliability – NEL HALT/HASS qualified for crystal oscillator start-up conditions
- Fast Rise and Fall times
- Low cost
- COTS/Dual use

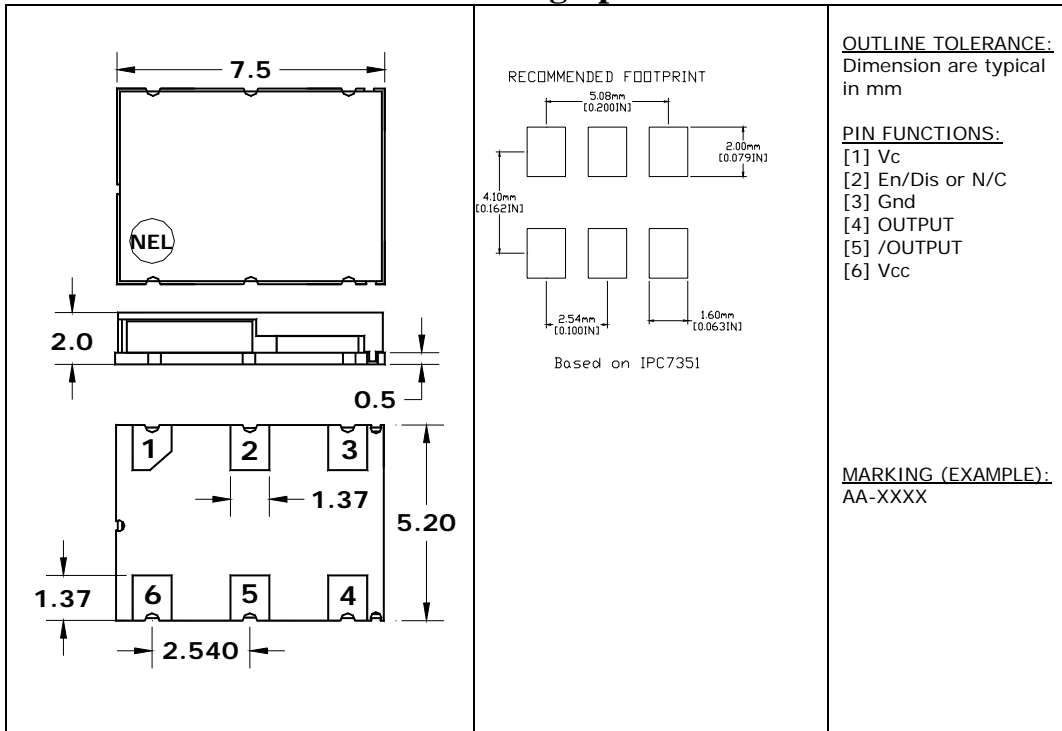
Creating a Part Number



AA-A3DDXXX-X Series

Rev. F

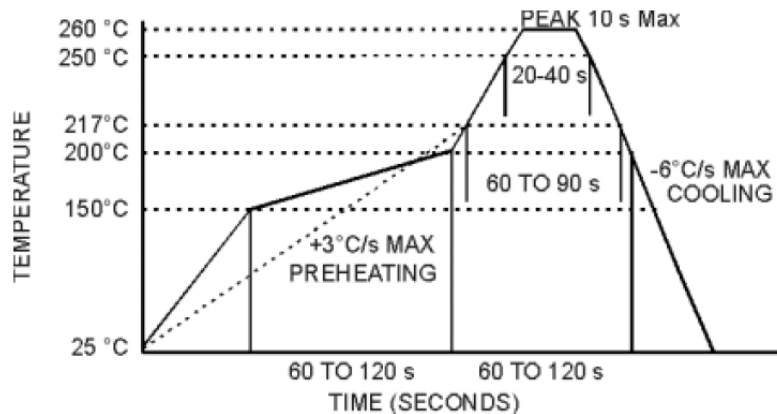
Drawing Specification



Environmental and Mechanical Characteristics

Operating temp. Range	see part # table
Mechanical Shock	Per MIL-STD-202, Method 213, Cond. A
Thermal Shock	Per MIL-STD-883, Method 1011, Cond. A
Vibration	Per MIL-STD-883, Method 2007, Cond. A
Hermetic Seal	Leak rate less than 1×10^{-8} atm.cc/s of helium, crystal only.
Soldering conditions	See MAX reflow profile below; The device may be reflowed once. Reflowing upside down is not allowed. NO CLEAN assembly is recommended.

MAX Reflow Profile



The device may be reflowed once. Reflowing upside down is not allowed. NO CLEAN assembly is recommended.

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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Operating Temperature Range	To	-40 to +85	°C
Storage Temperature Range	Tst	-50 to +90	°C
Supply Voltage	Vcc	-0.5 to 5.5	V
Control Voltage	Vc	-0.5 to 5.5	
Enable/Disable Voltage	Ven/dis	0 to Vcc	V

Electrical Parameters

Parameter	Symb	Conditions, Note	MIN	TYP	MAX	Unit	
Nominal Frequency	Fo		1		260	MHz	
Supply Voltage	Vcc	Code A	3.135	3.3	3.465	V	
Supply current	Icc			60	80	mA	
Output Logic Type				LVDS			
Load		At receiving end between the outputs	90	100	110	Ohm	
Output Levels	Vod	Differential amplitude	247	330	454	mV	
		Amplitude error			50	mV	
	Vof	Offset Voltage	1.125	1.25	1.375	V	
		Offset voltage error			50	mV	
Duty Cycle (Symmetry)		At outputs crossing, room temperature	45/55	50/50	55/45	%	
Rise/Fall Time	Tr/Tf	20 to 80, 80 to 20 %		0.5	0.7	ns	
Jitter	Integrated	J	Integrated from Phase Noise, 12 KHz to 20 MHz, RMS 100Hz to 80KHz,RMS		0.1	0.2	ps
						1.0	ps
					0.3	ps	
	Wavecrest characterized		Random period,		2.5		ps
			Accumul., pk-to-pk		17		ps
		Determin.	F>52 MHz	6		ps	
Sub-harmonics		F > 52 MHz		-50	-42	dBc	
Phase Noise	£(Δf)	155.52 MHz, @ 10 Hz @100 Hz @1 KHz @10KHz @100KHz @>1MHz		-70 -100 -125 -140 -145 -145		dBc/Hz	
Frequency Stability, usually not specified – unless necessary, APR is specified to incorporate stability	ΔF/F	Overall, including temperature, aging 10 years, shock and vibration @Vc=Vcc/2; APR 50 ppm, or less	±20	±30		ppm	
Control Voltage Range	Vc		0V		Vcc	V	
Setability	Vcs	Vc to set the F at Fo; T, Vcc, load – nominal, as shipped	0.4 Vcc	0.5 Vcc	0.6 Vcc	V	
Absolute Pull Range	APR	Over all conditions, see part # creation	20, 32, 50, 100			ppm	
Input impedance	Zin	@ Fmod < 100 KHz	50			KOhm	
Modulation Bandwidth		At Vc = Vcc/2, -3dB	20			KHz	
Enable		Pin 2 = Low, 0 to Vcc-1.62 V, or floating	Enabled			V	
Disable		Pin 2 = High, Vcc-1.025 V to Vcc	Disabled, Pin4 = Logic “1”, Pin5 = Logic “0”			V	