AE-X0A5XXXX-X Series
SINEWAVE/CMOS HF XO

Rev. G

Description

The AE-X0A5XXXX Series of crystal oscillators (XO) provides high frequency with Sine-Wave or CMOS output. The device provides exceptionally low Phase Noise and Jitter. It's packaged in a miniature, FR-4 based 17x14 mm SMD package.

Applications and Features

- Frequency Synthesizers, Low Phase Noise Reference
- High Reliability – NEL HALT/HASS qualified for crystal oscillator start-up conditions
- Extremely Low Phase Noise and Jitter
- SONET ± 20 ppm overall free-run stability available
- High Shock Resistance, to 1000g
- COTS/Dual use

Creating a Part Number

AE- X 0A5 X X X X - X - FREQ

Package code
AE – 8 pad 17x14 mm SMD

Operating Voltage
0 - 5.0 V ± 5%
A - 3.3 V ± 5%

Output
C - CMOS
S - Sinewave

Technique
M - Multiplied
N - Straight

Temperature Range, °C
A – 0 to 50
B - 0 to 70
C - -20 to 70
D - -40 to 85
9 – customer specific

Frequency Stability, ppm
E - ±20
F – ±25
G – ±50
H – ±100
9 – Customer specific

Environmental
L Contains a level of lead that is in excess of RoHs directive and is not designed for reflow
R RoHS compliant

NEL FREQUENCY CONTROLS, INC.
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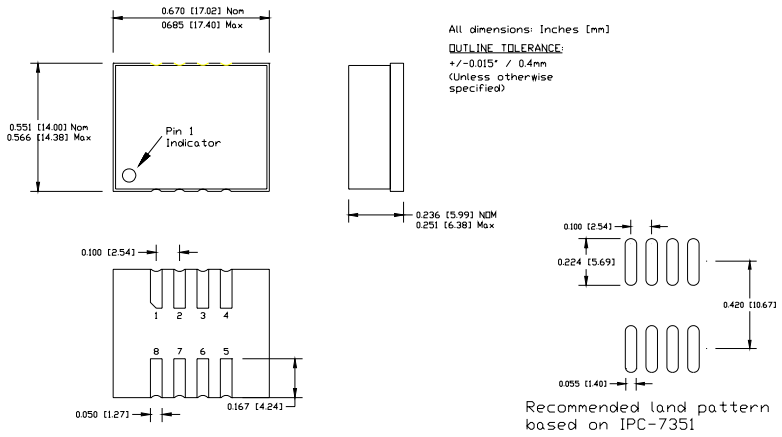
Drawing Specification



OUTLINE TOLERANCE:
±0.015" / 0.4mm
(Unless otherwise specified)

PIN FUNCTIONS:
[1] Vcc
[2] [3] [4] [7] - GND
[5] OUTPUT
[6] N/C or GND
[8] N/C

MARKING (EXAMPLE):
AE-XXXX

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Operating Temperature Range	To	-40 to +85	ºC
Storage Temperature Range	Tst	-50 to +90	ºC
Supply Voltage	Vcc	-0.5 to 5.5	V

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Electrical Parameters (1)

Parameter		Symb	Conditions, Note		MIN	TYP	MAX	Unit
Nominal Frequency		Fo	See Note below		12		250	MHz
Supply Voltage		Vcc	Code 0 Code A		4.75 3.135	5.0 3.3	5.25 3.465	V
Supply current		Icc	No load, Vcc=3.3V 100MHz			60	160	mA
Output Logic Type			S version C version			Sine CMOS		
Load			Internally AC coupled		45	50	55	Ohm
Harmonic		Ph					-25	dBc
Sub-Harmonics			N version		None			
Sub-Harmonics			M version			-50	-45	dBc
Output Power		Po	S version Into 50 ohm,5V 3.3V		7 5	10 7		dBm
Logic Levels		Vol Voh	C version		0.9Vcc		0.1Vcc	V
Jitter	Integrated, RMS	J	Integrated from Phase Noise, 12 KHz to 20 MHz RMS			0.1	0.15	ps
			100Hz to 80KHz,RMS				0.5	ps
			50 KHz to 80 MHz			0.2		ps
	Wavecrest characterized		Random period,			2.5		ps
			Accumul., pk-to-pk			17		ps
			Determin.	N version		0		ps
				M version @ 100MHz		10		
Phase Noise, N version		£(Δf)	100 MHz, 3.3V	@ 10 Hz @100 Hz @1 KHz @10KHz @100KHz @>1MHz		-85 -115 -145 -170 -172 -175	-80 -110 -140 -168 -170 -172	dBc/Hz
Phase Noise, M version, Sinewave only		£(Δf)	100 MHz, 3.3V	@ 10 Hz @100 Hz @1 KHz @10KHz @100KHz @>1MHz		-95 -125 -145 -160 -162 -165	-90 -120 -140 -158 -160 -162	dBc/Hz
Frequency Stability, overall conditions		ΔF/F	See chart			±50		ppm

Note 1. All parameters, unless otherwise specified, are at nominal conditions, ie: T=25°C, Nominal Vcc & Nominal Load.

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Typical Phase Noise at 100 MHz

AE-X0A5NXXX "N" Non-multiplied version

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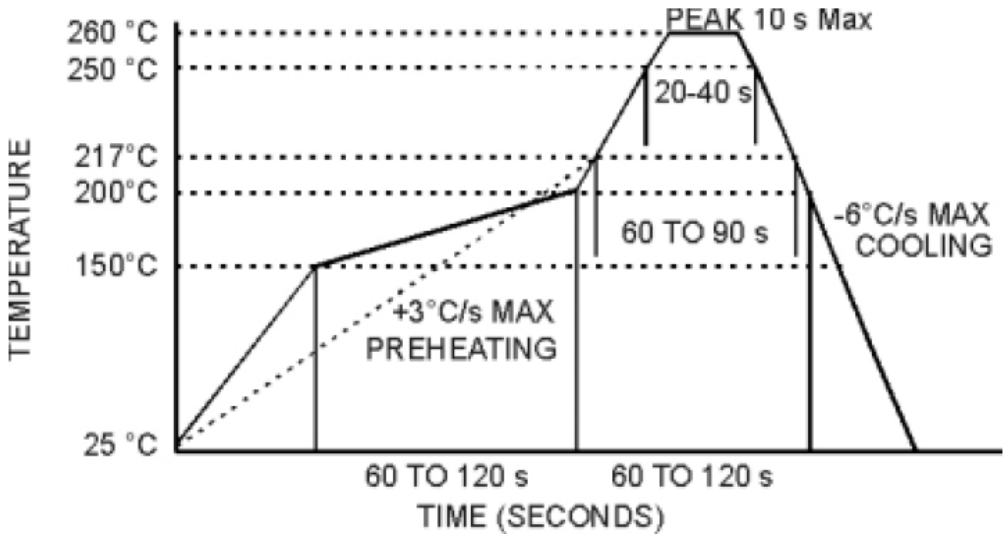
Environmental and Mechanical Characteristics

Operating temp. range	see part # table
Mechanical Shock	Per MIL-STD-202, Method 213, Cond. A
Thermal Shock	Per MIL-STD-883, Method 1011, Cond. A
Vibration	Per MIL-STD-883, Method 2007, Cond. A
Hermetic Seal	Leak rate less than $5x10^{-8}$ atm.cc/s of helium , crystal only.
Soldering conditions	See MAX reflow profile below; The device may be reflowed once. Reflowing upside down is not allowed. NO CLEAN assembly is recommended.

MAX Reflow Profile



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