

AP-XX57XXX-X Series Multiple outputs

Rev. E

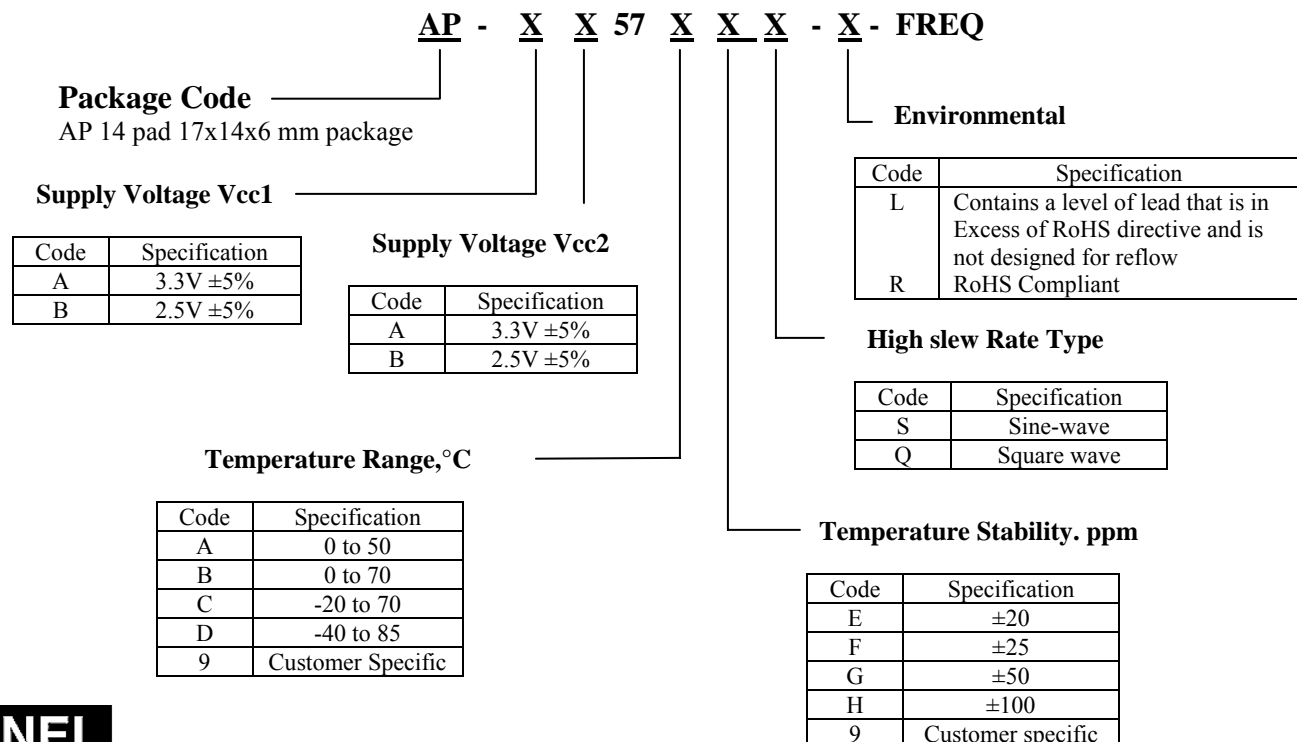
For use with High Bandwidth analog-to-digital converters (ADC) and digital-to-analog converters (DAC)

Description The **AP-XX57XXX-X Series** of crystal oscillators (XO) provides high frequency multiple synchronous clocks, including AC coupled high slew rate square-wave (or sine-wave) differential pair for ADC/DAC; differential PECL; and LVDS outputs. Logic outputs can be referenced to 2 different supply voltages. The device provides exceptionally low Phase Noise and Jitter.

Applications and Features

- High speed Analog-to-Digital Converter clock source
- High slew rate waveform edges minimize the slope dependent ADC jitter and ADC uncertainty
- Synchronous Logic Outputs for FPGA or other system needs clocks
- Output characterized to match specified ADC or DAC clock input conditions
- Ideal for use with high bandwidth ADC and DAC Applications
- Lowest Jitter Solution - Exceptionally low phase noise reference and ultra low jitter clock source
- High reliability – NEL HALT/HASS qualified for crystal oscillator start-up conditions
- Extremely low phase noise and jitter
- High shock resistance, to 1000g
- COTS/Dual use

Creating a Part Number



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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Operating Temperature Range	To	-40 to +85	°C
Storage Temperature Range	Tst	-50 to +90	°C
Supply Voltage	Vcc1, Vcc2	-0.5 to 5.5 (5V) -0.5 to 3.6 (2.5 and 3.3V)	V

Electrical Parameters

Parameter	Symb	Conditions, Note	MIN	TYP	MAX	Unit	
Nominal Frequency	Fo		10		500	MHz	
Supply Voltage	Vcc1, Vcc2	Code A Code B	3.135 2.375	3.3 2.5	3.465 2.625	V	
Supply current	Icc	Total			200	mA	
Output Logic Type	QH, QHN	AC coupled, code "Q"		Differential Square Wave			
	QH, QHN		AC coupled, code "S"		Differential Sine Wave		
	QP, QPN			DPECL			
	QL, QLN			LVDS			
Load	QH, QHN	Per ADC or DAC specification					
	QP, QPN	50 Ohm to Vcc-2V DC or Thevenin equivalent					
		100 Ohm between the outputs at receiving end					
Output Levels	QH, QHN	Vod	1.0	1.5	2.0	V	
	QP, QPN		Standard PECL 100				
	QL, QLN		Standard LVDS				
Slew Rate	QH, QHN	At 50% of output voltage swing	1.8	2.0		V/ns	
Jitter	Integrated, QH, QHN; QP, QPN outputs	J	Integrated from Phase Noise, 12 KHz to 20 MHz, RMS	250MHz	0.1	0.15	ps
			Deterministic, Peak-to-peak	500MHz	0.14	0.2	
				500MHz	4		
Sub-harmonics		**	F>250 MHz	-50	-45	dBc	
Phase Noise	£(Δf)	250 MHz, QN, QHN; QP, QPN	@ 10 Hz	-50	-45	dBc/Hz	
			@ 100 Hz	-80	-75		
			@ 1 KHz	-120	-110		
			@ 10KHz	-150	-140		
			@ 100KHz	-152	-152		
			@ >1MHz	-152	-152		
Phase Noise	£(Δf)	500MHz, QN, QHN; QP, QPN	@ 10 Hz	-60	-55	dBc/Hz	
			@ 100 Hz	-90	-85		
			@ 1 KHz	-118	-113		
			@ 10KHz	-135	-130		
			@ 100KHz	-140	-135		
			@ >1MHz	-145	-140		
Frequency Stability	ΔF/F	Overall, including temperature, aging 10 years, shock and vibration		±50	±100	ppm	

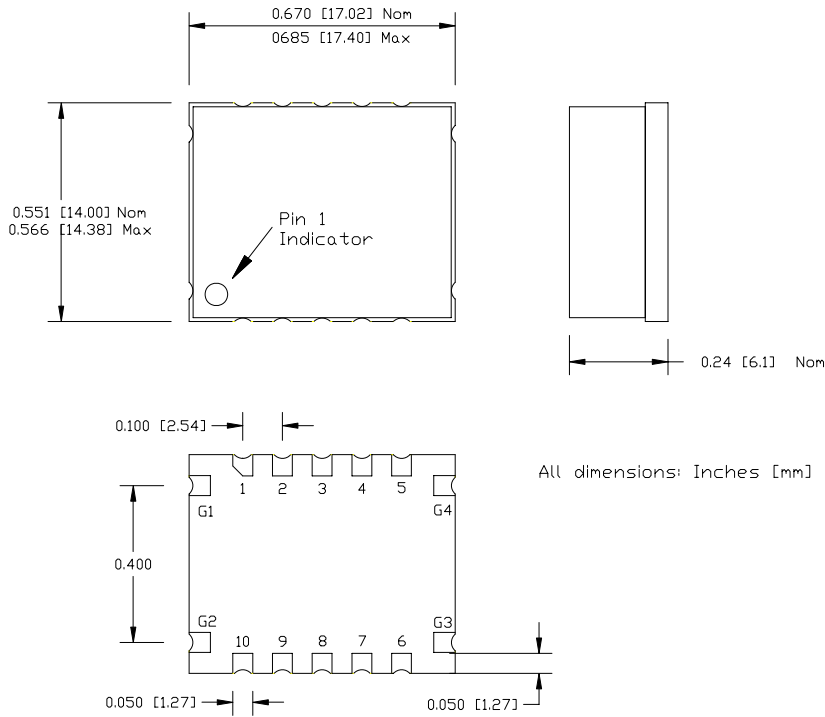


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Environmental and Mechanical

Operating temp. range	See creating a p/n chart
Mechanical Shock	Per MIL-STD-202, Method 213, Cond. E
Thermal Shock	Per MIL-STD-883, Method 1011, Cond. A
Vibration	Per MIL-STD-883, Method 2007, Cond. A
Soldering Conditions	See reflow profile; The device may be reflowed once. Reflowing upside down is not allowed. NO CLEAN assembly is recommended.
Hermetic Seal	Leak rate less than 5×10^{-8} atm.cc/s of helium , crystal only

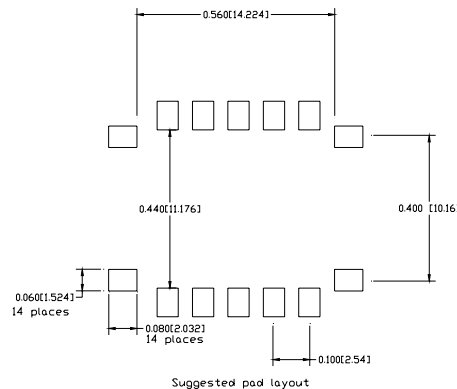


OUTLINE TOLERANCE:
 $\pm 0.015'' / 0.4\text{mm}$
 (Unless otherwise specified)

PIN FUNCTIONS

- [1] Vcc2⁽¹⁾
- [2] Reserve
- [3] EN⁽²⁾
- [4] QL (LVDS)
- [5] QLN
- [6] QHN (High Swing AC - coupled)
- [7] QH
- [8] QPN (PECL)
- [9] QP
- [10] Vcc1⁽¹⁾
- [G1-G4] GND

MARKING (EXAMPLE):
 XX-XXXX



- 1) V_{CC1} & V_{CC2} are connected internally
- 2) Negative Enable for LVDS outputs, consult factory for PECL & high slew rate options.

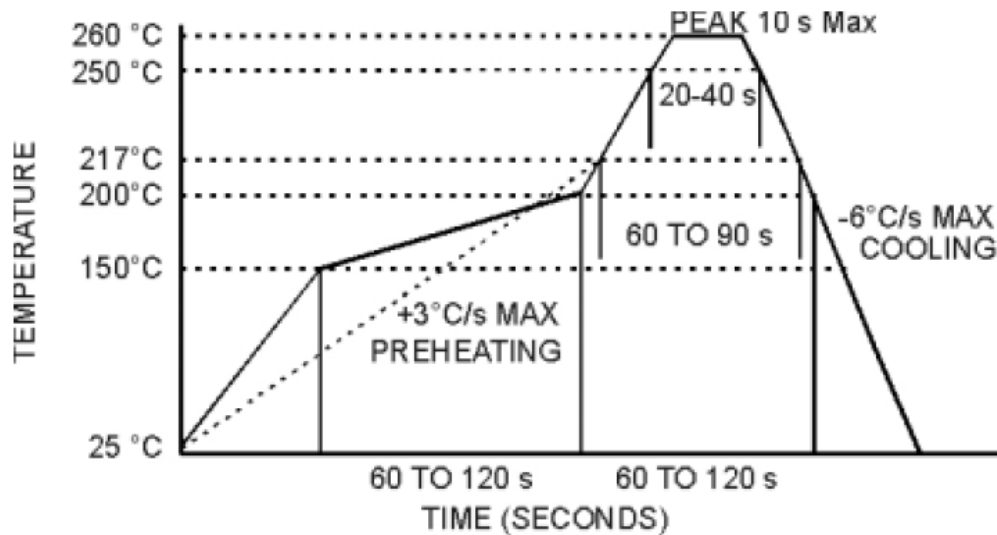


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Notes:

* This spec is preliminary and could be addressed on the case by case basis. Since different ADC/DAC have different requirements and different input impedances – this spec along with output impedance on QH/QHN would vary for particular custom requirement.

** Usually, to achieve frequency higher than 250 MHz Low Noise analog multiplication technique is used. As a rule the multiplication factor is odd number. If the frequency of sub-harmonic and its multiples is important for the application, customer is encouraged to specify multiplication factor for $F > 250$ MHz.

Maximum solder reflow profile

The device may be reflowed once. Reflowing upside down is not allowed. NO CLEAN assembly is recommended.