

**AA-ASCCXX-X Series**

**Rev. A**

**PATENT PENDING**

**Description**

The **Signal Conditioning Circuit (SCC)** is intended for use in the system, which requires multiple clocks in different nodes of the system to run synchronously in frequency **without master clock** along with SXO ensemble per 0934A. It takes the input signal from one of the synchronization buses and converts/translates it into differential (complementary) output signal with logic type specified by the customer: PECL, LVDS, or HCSL compatible. It covers the frequency range of 25 MHz to 160 MHz. Device is packaged in 7.5x5x2 mm FR4 based SMD package with 6 gold plated pads.

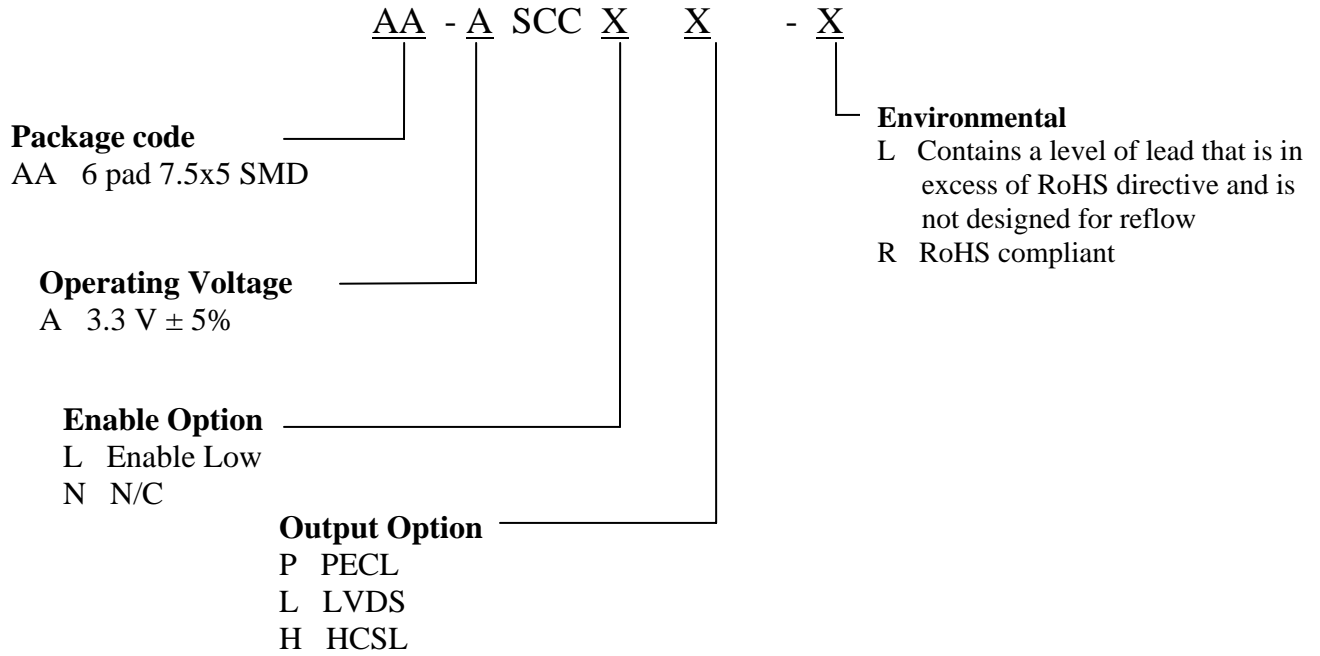
**Applications and Features for SXO ensemble with SCC**

- Unlimited scalability/easily expandable
- Ideal for blade applications
- Provides a complete, system-wide clock redundancy solution
- High reliability systems with multiple synchronous clocks.
- Greatly improved system reliability
- Low Phase Noise and jitter
- No master clock, no PLL required for the system
- Eliminates additive jitter degradation associated with clock distribution
- “Hot” – swappable
- Synchronize independent of power application sequence/No special power sequence required
- Improves Phase jitter at every node
- While in sync all units exhibit identical phase noise characteristics
- Low cost
- COTS/Dual use

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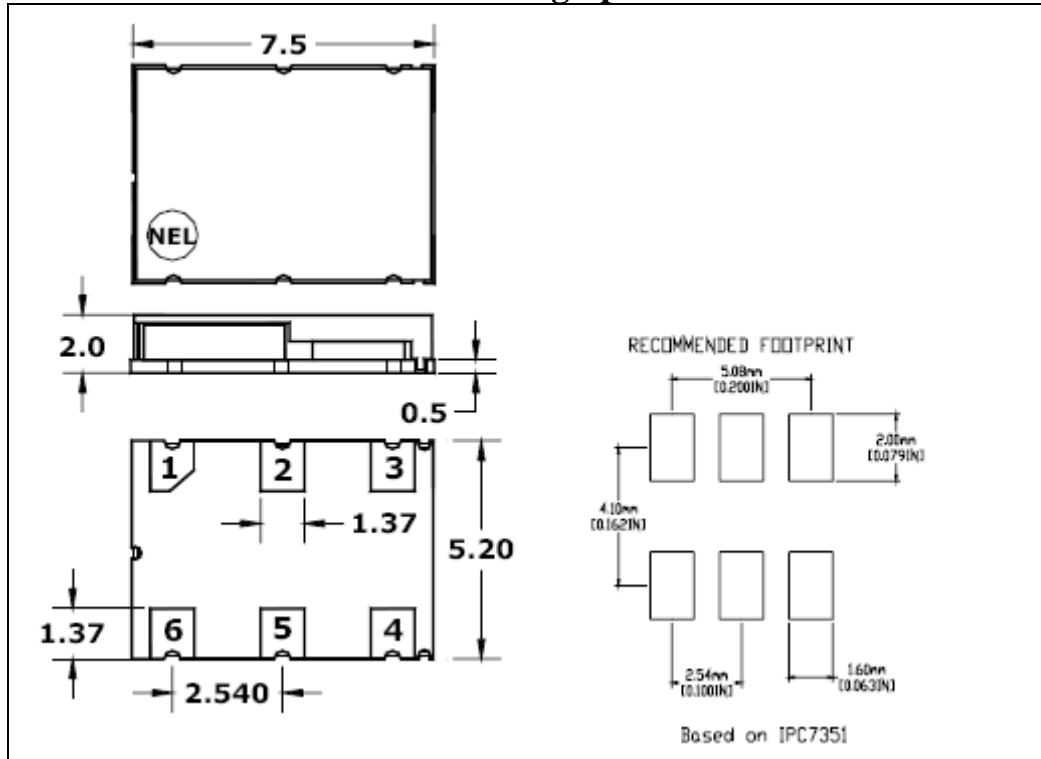
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Creating a Part Number



Note: En/Dis feature may not be available with LVDS output

**Drawing Specification**



**Electrical Connections**

Pin out	Pin 1=Input; Pin 2=Optional EN/DIS or N/C; Pin 3=GND; Pin 4=Output; Pin 5= Complementary Output; Pin 6= Vcc
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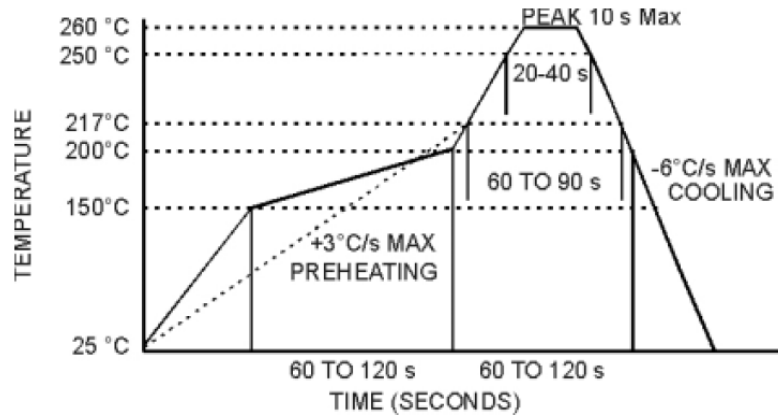
**Environmental and Mechanical Characteristics**

<b>Operating temp. Range</b>	-40°C to 85°C
<b>Mechanical Shock</b>	Per MIL-STD-202, Method 213, Cond. A
<b>Thermal Shock</b>	Per MIL-STD-883, Method 1011, Cond. A
<b>Vibration</b>	Per MIL-STD-883, Method 2007, Cond. A
<b>Soldering conditions</b>	See MAX reflow profile below

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### MAX Reflow Profile



### Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Operating Temperature Range	To	-40 to +85	°C
Storage Temperature Range	Tst	-50 to +90	°C
Supply Voltage	Vcc	-0.5 to 3.6	V
Enable/Disable Voltage	Ven/dis	0 to Vcc	V
Input Voltage Amplitude	Vin	Vcc	V

### Electrical Parameters

Parameter	Symb	Conditions, Note	MIN	TYP	MAX	Unit	
Nominal Frequency, Differential Outputs	Fo		25		160	MHz	
Supply Voltage	Vcc		3.135	3.3	3.465	V	
Supply current	Icc	Loaded both outputs, 100 MHz		40	60	mA	
LVDS OUTPUT	Load	At receiving end between the outputs	90	100	110	Ohm	
	Output Levels	Vod	Differential amplitude	247	330	454	mV
			Amplitude error			50	mV
		Vof	Offset Voltage	1.125	1.25	1.375	V
			Offset voltage error			50	mV
Duty Cycle (Symmetry)		At outputs crossing, room temperature	45/55	50/50	55/45	%	
Rise/Fall Time	Tr/Tf	20 to 80, 80 to 20 %		0.3	0.5	ns	
LVPECL OUTPUT	Load	Output to Vcc-2V, or Thevenin Equivalent		50		Ohm	
	Output Levels	Voh	overall	Vcc-1.025			V
		Vol				Vcc-1.620	
Duty Cycle		At 50% of output	45/55	50/50	55/45	%	



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	(Symmetry)		voltage swing				
	Rise/Fall Time	Tr/Tf	20 to 80, 80 to 20 %		0.3	0.5	ns
<b>HCSL OUTPUT</b>	Load		At receiving end each output, Rs = 0 Ohm		50		Ohm
	Output Levels	Voh	Output High 1,2	600	700	850	mV
		Vol	Output Low 1,2	-150	0	150	V
		Vcr	Crossing Point	250	350	550	mV
	Duty Cycle (Symmetry)		At outputs crossing, room temperature	45/55	50/50	55/45	%
	Rise/Fall Time	Tr/Tf	From 0.175 to 0.525 V		0.35	0.5	ns
Input signal	Vin	Peak-to-peak	1.0		Vcc	V	
Enable		Pin 2 = Low, 0 to Vcc-1.62 V, or floating	Enabled			V	
Disable, see note 1.		Pin 2 = High, Vcc-1.025 V to Vcc	Disabled, Pin4 = Logic "1", Pin5 = Logic "0"			V	
Skew		Unit to unit			2	Degrees	

Notes

1. En/Dis is not available with LVDS output. Please contact factory on different polarity of En/Dis control.