

SU-X29PXXX-X Series PECL/LVPECL UHF XO

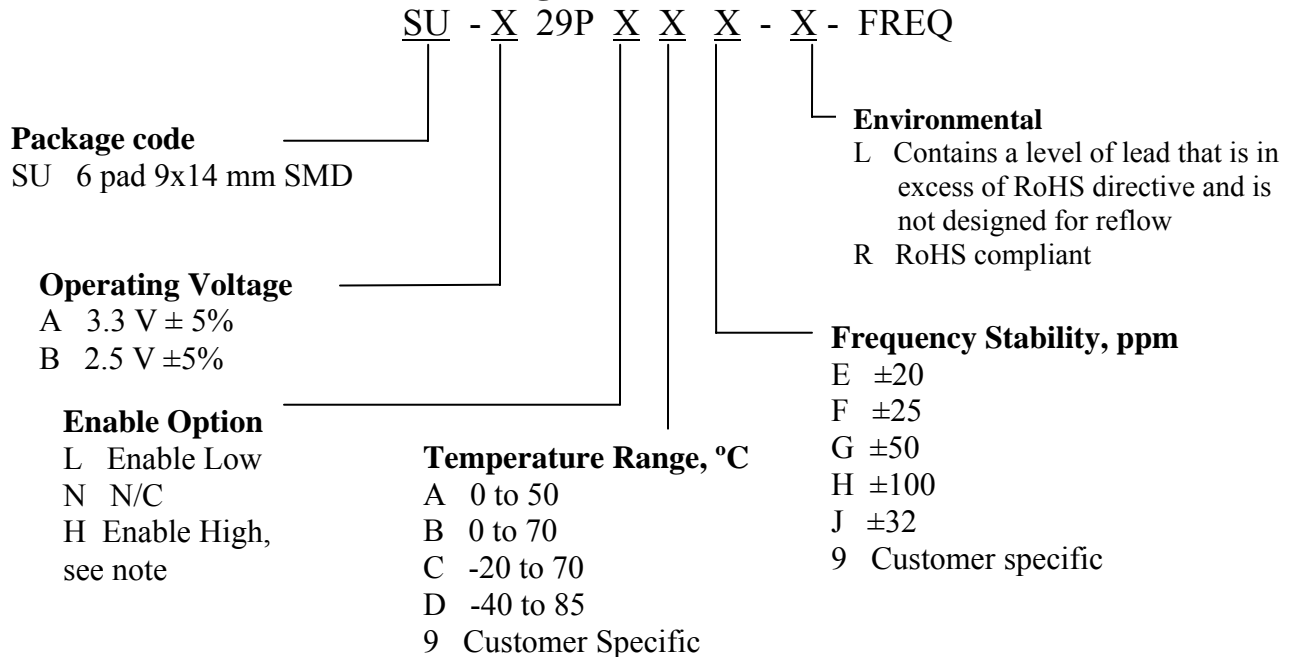
Description

The **SU-X29PXXX Series** of crystal oscillators (XO) provides ultra high frequency with PECL/LVPECL complementary outputs. The outputs can be disabled for test automation or combining multiple clocks. The device is based on low noise analog harmonic frequency multiplication, providing exceptionally low Phase Noise and Jitter. It's packaged in a miniature, FR-4 based 9x14 mm SMD package

Applications and Features

- Fiber Channel; 10 GbE; Infiniband; Network Processors; SONET/SDH
- High Reliability – NEL HALT/HASS qualified for crystal oscillator start-up conditions
- Ultra Low Phase Noise and Jitter
- Frequency Range to 1,800 MHz
- SONET ± 20 ppm overall stability available
- High Shock Resistance, to 1000g
- COTS/Dual use

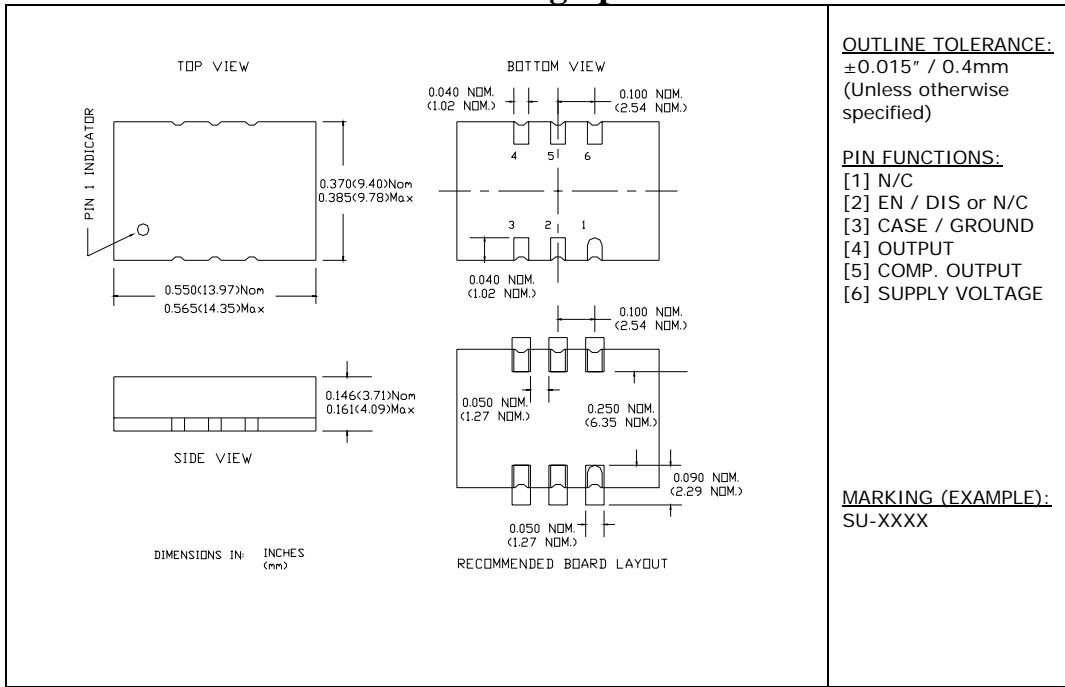
Creating a Part Number



SU-X29PXXX-X Series

Rev. F

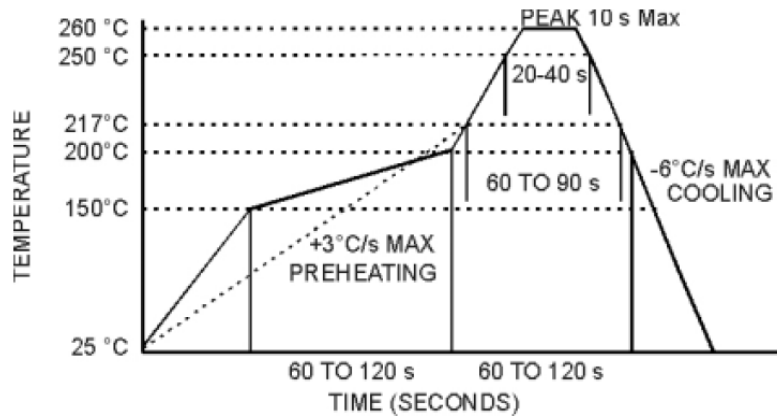
Drawing Specification



Environmental and Mechanical Characteristics

Operating temp. range	see part # table
Mechanical Shock	Per MIL-STD-202, Method 213, Cond. A
Thermal Shock	Per MIL-STD-883, Method 1011, Cond. A
Vibration	Per MIL-STD-883, Method 2007, Cond. A
Hermetic Seal	Leak rate less than 1×10^{-8} atm.cc/s of helium, crystal only.
Soldering conditions	See MAX reflow profile below; The device may be reflowed once. Reflowing upside down is not allowed. NO CLEAN assembly is recommended.

MAX Reflow Profile



The device may be reflowed once. Reflowing upside down is not allowed. NO CLEAN assembly is recommended.

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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Operating Temperature Range	To	-40 to +85	°C
Storage Temperature Range	Tst	-50 to +90	°C
Supply Voltage	Vcc	-0.5 to 4.5	V
Enable/Disable Voltage	Ven/dis	0 to Vcc	V

Electrical Parameters

Parameter	Symb	Conditions, Note	MIN	TYP	MAX	Unit
Nominal Frequency	Fo	At Vcc=2.5V, Fmax is 1.6 GHz	200		1,800	MHz
Supply Voltage	Vcc	Code A Code B	3.135 2.375	3.3 2.5	3.465 2.625	V
Supply current	Icc			110	130	mA
Output Logic Type				LVPECL		
Load		Output to Vcc-2V, or Thevenin Equivalent		50		Ohm
Output Levels	Voh Vol	Overall, at F > 1.0 GHz output swing may deteriorate, consult factory	Vcc-1.025		Vcc-1.620	V
Duty Cycle (Symmetry)		At 50% of output voltage swing	45/55	50/50	55/45	%
Rise/Fall Time	Tr/Tf	20 to 80, F < 1GHz 80 to 20 % F > 1 GHz		0.4 0.2	0.5 0.3	ns
Jitter*	Integrated	J Integrated from Phase Noise, 12 KHz to 20 MHz, RMS 100Hz to 80KHz,RMS 50 KHz to 80 MHz		0.1	0.2	ps
					1.0	ps
				0.3		ps
	Wavecrest characterized	Random period, Accumul., pk-to-pk Determin.		2.5		ps
				36		ps
				6	12	ps
Phase Noise*	£(Δf)	622.080MHz @ 10 Hz @100 Hz @1 KHz @10KHz @100KHz @>1MHz		-60 -90 -118 -135 -140 -145	-55 -85 -113 -130 -135 -140	dBc/Hz
Sub-harmonics		At 622.08 MHz		-50	-46	dBc
Frequency Stability	ΔF/F	Overall, including initial calibration, temperature, aging 10 years, shock and vibration			From ±20, see table for part number	ppm
Enable		Pin 2 = Low or floating, 0 to Vcc-1.62 V	Enabled			V
Disable		Pin 2 = High, Vcc-1.025 V to Vcc	Disabled, Pin4 = Logic "1", Pin5 = Logic "0"			V

Enable High (CMOS level) at F < 650 MHz available, consult factory

Notes:

1. * Phase noise and phase jitter are frequency dependent. Phase noise deteriorates approximately $20\log N$ ("N" if frequency ratio) with rising the frequency. Please consult factory for detailed Phase Noise and Phase Jitter characterization at your frequency of interest.
2. All parameters, unless noted otherwise are specified for nominal conditions, i.e. ambient temperature is 25 °C, Vcc – nominal.