

Rev.A

V-AN-XXYY-XX -100.000 MHz Phase-Locked Clean-up ULPN VCXO with Low G-sensitivity

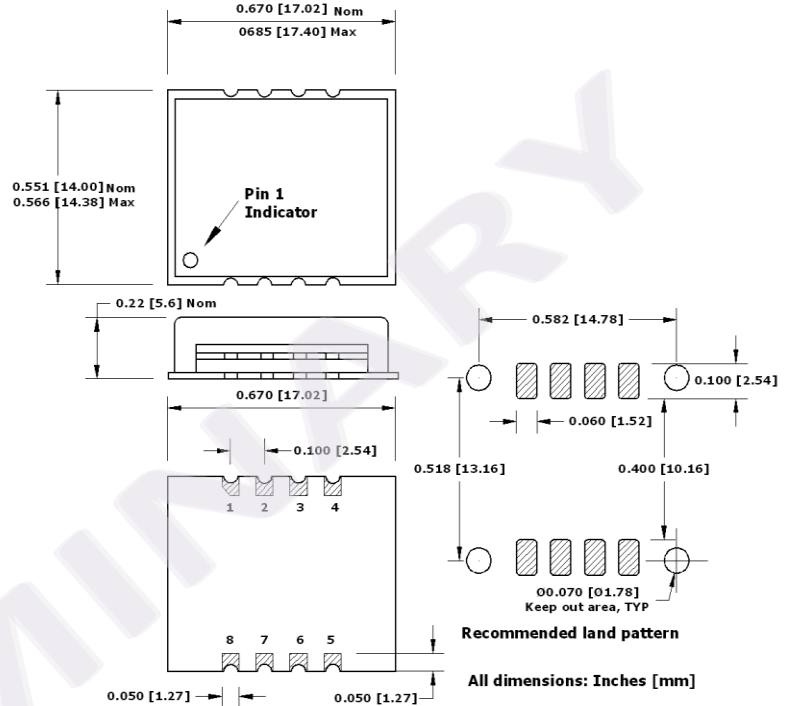
Product Data Sheet

Features

- Low G-sensitivity
- Low Phase Noise Similar to OCXO
- Compact SMD Package
- Low Power Consumption Independent on Ambient Temperature and no Warm-up
- Fast Ready

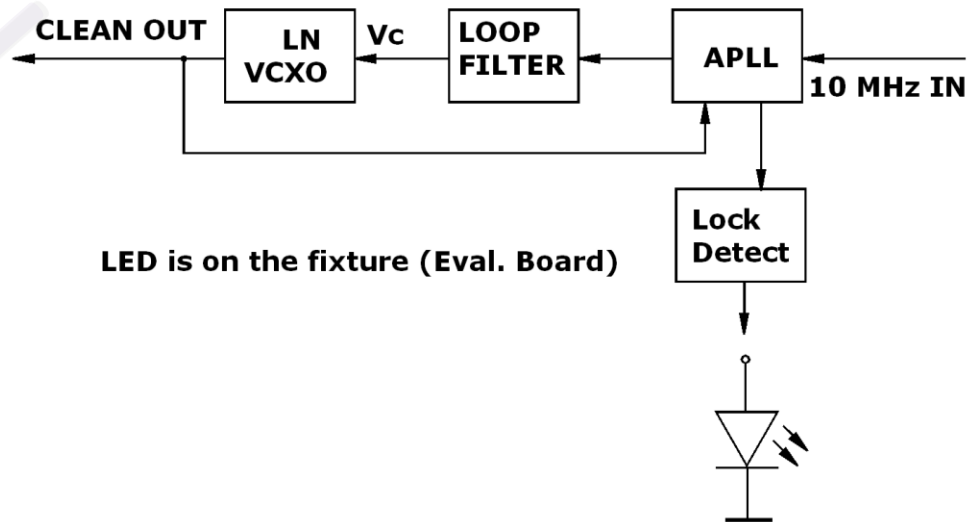
Applications

- Significantly improves Phase Noise of incoming signal
- Atomic Clocks, GNSS Based Clocks
- Test and Measurement
- COTS/Dual use



Pinout

- Pad #1 - Vcc
- Pad #2 - GND
- Pad #3 - GND
- Pad #4 - GND
- Pad #5 - RF OUT
- Pad #6 - Do Not Connect
- Pad #7 - 10 MHz In
- Pad #8 - Lock Detect



**FREQUENCY
CONTROLS, INC.**

357 Beloit Street, Burlington, WI 53105 U.S.A. Phone 262/763-3591 FAX 262/763-2881

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Specifications:

Parameter	Symb	Condition	Min	Typ	Max	Unit	Note
Absolute Maximum Ratings							
Input Break Down Voltage	V _{cc}		-0.5		5.5	V	V _{cc} = 5 V
Operating Temp.	T _o		-20		70	°C	
Operable Temp.	T _O		-40		85	°C	
Storage temper.	T _s		-40		85	°C	

Electrical

Input Frequency	Fin			10.000 100.000		MHz	Option A Option B	All parameters for output frequency 100 MHz
Output Frequency	F _{out}		80	100.000	125	MHz		
Frequency Capture Range (APR)	ΔF/F	Overall	±100			ppb		
Allan Deviation		.01s to 1.0s		8E-11				
Frequency stability	ΔF/F	Locked	Equal to incoming signal					
Recommended MAX Input SSB Phase Noise	£(Δf)	10 Hz			-80	dBc/Hz	10 MHz, Option A	
		100 Hz			-110			
		1 KHz			-130			
		10 KHz			-140			
		100 KHz			-140			
		10 Hz			-70		100 MHz, Option B	
		100 Hz			-100			
		1 KHz			-120			
		10 KHz			-140			
		100 KHz			-140			
Input signal		CMOS	2			V	Swing	
		Sine Wave	0		5	dBm		
Output SSB Phase Noise Improvement Compared to Input Phase Noise		1 Hz		20		dBc/Hz	Cannot improve beyond listed above noise floor	
		10 Hz		40				
		100 Hz		50				
		1 KHz		50				
		10 KHz		50				
Output SSB Phase Noise Floor	£(Δf)	10 Hz		-95		dBc/Hz		
		100 Hz		-125				
		1 KHz		-152				
		10 KHz		-170				
		100 KHz		-172				
G-sensitivity		worst direction			±0.2	ppb/G		
Input Voltage	V _{cc}	Code 0	4.75	5.0	5.25	V	By special request	
		Code A	3.2	3.3	3.45			
Power consumption	P			100		mW	Driving 50 Ohm code S	
Spectral Purity		Subharmonics		-70	-50	dBc	Output Code S	
		Spurious			-80			
		Harmonics		-35	-30			
Load	Internally AC coupled 50 Ohm (Sinewave) 10K Ohm//15pf (CMOS/TTL)							
Lock Time				1		minute		
Output Power	P _{out}	Into 50 Ohm	9	11		dBm	Output Code S	
Logic 1 (CMOS)	V _{oh}		0.7V _{ref}			V	Output Code T	
Logic 0 (CMOS)	V _{ol}				0.1V _{ref}	V	Output Code T	
Duty Cycle			45/55		55/45	%	Output Code T	
Rise/Fall Time	Tr/Tf			4	5	ns	Output Code T	
Lock Detect			Logic "1"				Can drive LED	

Environmental and Mechanical

Operating temp. range	-20°C to 70°C Standard, Other options – see chart below
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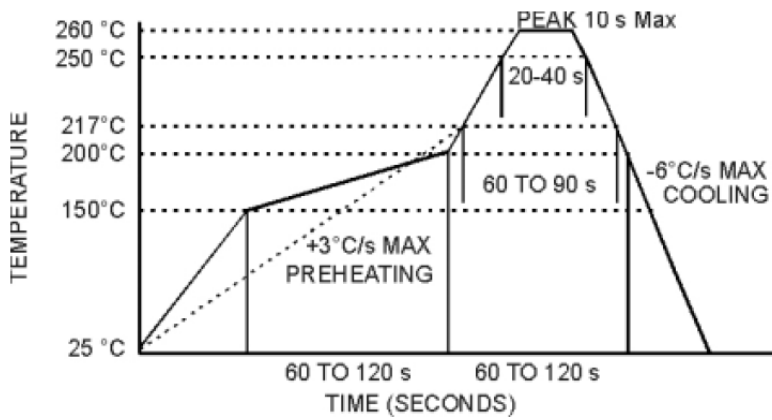


Mechanical Shock	Per MIL-STD-202, 30G, 11ms , survival
Vibration	Per MIL-STD-202, 5G to 2000 Hz, Survival
Soldering Conditions	See MAX reflow profile below; The device may be reflowed once. Reflowing upside down is not allowed. Hand soldering is highly encouraged. NO CLEAN assembly is recommended

Notes:

* All parameters, unless otherwise specified, are at nominal conditions, ie: T=25°C, Nominal Vcc & Nominal

MAX Reflow Profile



PRELIMINARY

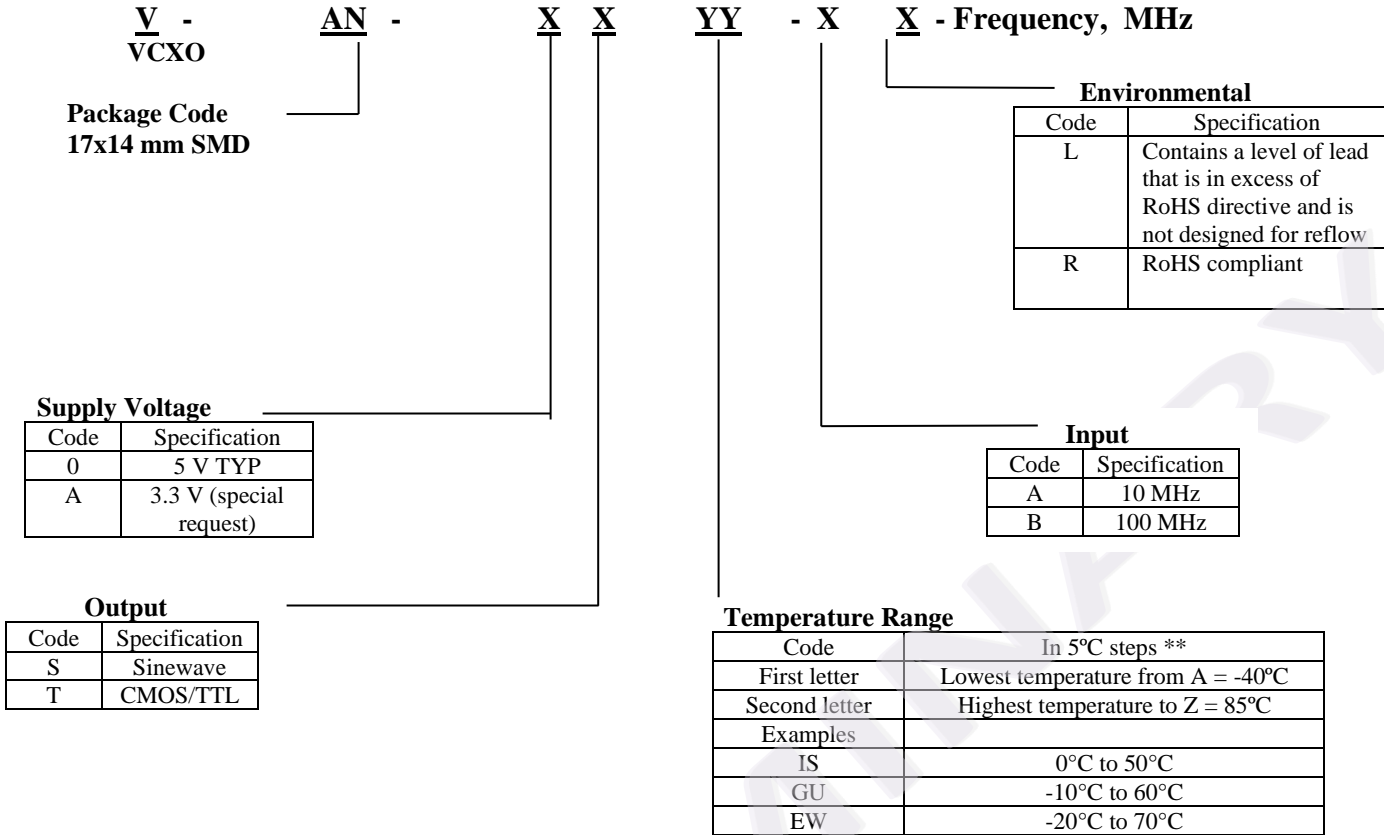


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Creating a Part Number



****Temperature Code Table**

Letter	Temp °C	Letter	Temp °C	Letter	Temp °C	Letter	Temp °C	Letter	Temp °C	Letter	Temp °C
A	-40	F	-15	K	10	P	35	U	60	Z	85
B	-35	G	-10	L	15	Q	40	V	65		
C	-30	H	-5	M	20	R	45	W	70		
D	-25	I	0	N	25	S	50	X	75		
E	-20	J	5	O	30	T	55	Y	80		

